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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,422	07/23/2004	Lars Skog	P16178-US1	8125

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EXAMINER	
MATIN, NURUL M	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/502,422	SKOG ET AL.	
	Examiner	Art Unit	
	Nurul M. Matin	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments see remarks, filed March 5, 2007 with respect to the rejection(s) of claim(s) 11, 13, 14 under 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tamura, US 2003/0042957 and Mosley et al, US 6597197.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 11, 12, 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura, US 2003/0042957 and in view of Doblar et al, US 6194969.

Re claim 1, A computer system clocking system, said system comprising (page 17, Para [0279]: at least two units with clock functionality (fig 43/#301, 302, page 17, Para [0279], line 4, master and slave (two units) the units being coupled to a common system clock line (fig.43, page 17, Para [0281], the reference clock is a common clock line), a common internal clock line (fig.43, page 17, Para [0281], internal clock line (314). But Tamura fails to disclose the following limitations. However, Dobler does

discloses a logic bus (fig3/#330, col.5, line 34-35," control bus 330"), wherein one unit is dedicated as a master unit at a time (col.3, line 19-23," if master unit fails then slave unit will take place as master unit"), the dedication of the master unit being dependent on at least a signal being given so as not to select a given unit for being a master unit (col.3, line 19-23, " master clock signal"), and if a given unit is dedicated as master unit when such a signal is given, the system performing a switchover causing another unit as the one not selected to be dedicated as master unit(col.3, line 23-26, col.1, line 49-52), each unit comprising: a clock source for generating a clock source signal, the clock source signal being adapted for being output on the internal clock line(fig3, col.5,line 42-45); and a phase lock loop device generating a signal, which is derived from the signal on the internal clock line and which is output on the system clock line if the unit is dedicated as master unit(fig.3, col.5, line 39-42, the select PLL 300 produces a clock signal synchronized with the appropriate input clock signal106" and also col.5, line 40-44), wherein one source clock signal of a unit is output on the internal clock line and all phase lock loop devices of all units generate phase lock loop output signals derived from the internal clock signal, the outputs of the phase lock loop devices being in phase with one another such that switchover from one phase lock loop output signal to another is seamless(col.2, line 25-27, col.5, line 65-col.6, line 3).

Therefore, taking the combined teaching of Tamura, Doblar as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the arrangement of the a logic bus, wherein one unit is dedicated as a master unit at a time, the dedication of the master unit being dependent on at least a signal being given so as not to select a

given unit for being a master unit, and if a given unit is dedicated as master unit when such a signal is given, the system performing a switchover causing another unit as the one not selected to be dedicated as master unit, each unit comprising: a clock source for generating a clock source signal, the clock source signal being adapted for being output on the internal clock line; and a phase lock loop device generating a signal, which is derived from the signal on the internal clock line, and which is output on the system clock line if the unit is dedicated as master unit, wherein one source clock signal of a unit is output on the internal clock line and all phase lock loop devices of all units generate phase lock loop output signals derived from the internal clock signal, the outputs of the phase lock loop devices being in phase with one another such that switchover from one phase lock loop output signal to another is seamless as thought in Doblar into Tamura to allow a phase-aligned slave clock to replace a master clock upon failure of the master clock.

Re claim 12, Tamura and Doblar references teach the system according to claim 11, and Tamura reference also teaches the unit dedicated as master unit generates the clock source signal on the internal clock line (fig.43).

Re claim 16, Tamura and Doblar references teach the system according to claim 11, and Doblar references also teaches the logic section of any unit comprises fault sense circuitry and wherein, if a fault is detected in any device, the system initiates switchover from a dedicated unit to a subsequent dedicated unit(col.6, line 54-63," the switching logic 430 determines that the input clock 106A has failed and automatically switches over to the redundant backup clock 106B").

Re claim 17, Tamura and Doblar references teach the system according to claim 11, Doblar reference also teaches an additional board not comprising any clock generating or clock evaluating functionality, the additional board being coupled to the system clock line but not to the internal clock line nor to the logic bus (fig.2, col.3, line 37-39, " an embodiment of two clock boards 105A and 105B and the coupling of their respective clock signals 106A and 106B and also system board 120").

3. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tamura, US 2003/0042957, Doblar et al, US 6194969 and in view of Mosley et al, US 6597197.

Re claim 13, Tamura and Doblar references teach the system according to claim 11, and Doblar reference also teaches each unit further comprises: a logic section communicating with the logic bus (col.5, line 36-38," the control bus (logic bus 330) provides a communications pathway between the system controller 110"). But they fail to disclose a first bidirectional port communicating with the internal clock line (col.2, line 21-22, " a first bidirectional data port operable at a first signal voltage level"); a second bidirectional port communicating with a system clock line, the logic section of the unit controlling the first and second bidirectional ports to input or output respective system clock signals and respective internal clock signals via enable signals (col.2, line 22-32, which discloses a second bidirectional port and also a system control circuit).

Therefore, taking the combined teaching of Tamura, Doblar and Mosley, as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the

arrangement of the a first bidirectional port communicating with the internal clock line; a second bidirectional port communicating with a system clock line, the logic section of the unit controlling the first and second bidirectional ports to input or output respective system clock signals and respective internal clock signals via enable signals as thought in Mosley into Tamura and Doblar so that the first data and clock ports can communicate with a first serial bus and the second data and clock ports can communicate with a second serial bus.

Re claim 14, Tamura, Dobler and Mosley references teach the system according to claim 13, and Dobler reference also teaches the enable signals(could be any signals) first change state when the system clock is in a logic state (switching logic) with a certain predetermined security time interval from state changes of the system clock (col.6,"line 50-53, col.5, line 51-53, where clock signal for synchronization of timing means predetermined security time").

Re claim 15, Tamura, Dobler and Mosley references teach the system according to claim 13, and Dobler reference also teaches the logic section, in cooperation with other logic sections of other units, negotiates a priority scheme according to which a predetermined order for dedicating units is determined(col.6, line 54-57, " the switching logic 430 determines that the input clock 106A has failed and automatically switches over to the redundant backup clock 106B means logic section in master unit and logic section in slave unit is cooperative).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nurul M. Matin whose telephone number is 571-270-1188. The examiner can normally be reached on mon-fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nurul Matin

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER